Application Note
Temperature Sensor IC
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Application Note
Temperature Sensor IC

1. **TSic™ 206/203/201/306/316/303/301**

The TSic™ series of temperature sensor ICs are specifically designed as a low-power solution for temperature measurement in building automation, medical/pharma technologies, industrial and mobile applications. The TSic™ provides a simple temperature measurement and achieves outstanding accuracy combined with long term stability.

The TSic™ has a high precision bandgap reference with a PTAT (proportional-to-absolute-temperature) output, a low-power and high-precision ADC and an on-chip DSP core with an EEPROM for the precisely calibrated output signal. The TSic™ temperature sensor is fully calibrated, meaning no further calibration effort is required by the customer.

Extended long wires (> 10 m) will not influence the accuracy. The TSic™ is available with digital (ZacWire, TSic™ x06), analog (0 V to 1 V, TSic™ x01) or ratiometric (10 % to 90 % V+, TSic™ x03) output signal. The low power consumption of about 35 µA makes it suitable for many applications.

With an accuracy of ±0.3 K in a temperature range of 80 K (e.g. +10 °C to +90 °C), the TSic™ sensors are more accurate than a class F0.3 (DIN EN 60751) platinum sensor. The tolerances of the TSic™ and DIN B and DIN A platinum sensors are compared in Figure 1. With a standard calibration, the TSic™ 30x is more accurate than a DIN B platinum sensor in the range of +10 °C to +110 °C. The range can be shifted up or downwards to reach a high accuracy between e.g. -30 °C to +50 °C.

### Output examples

<table>
<thead>
<tr>
<th>Temp (°C)</th>
<th>Digital Values (TSic x06)</th>
<th>Analog 0 V to 1 V (TSic x01)</th>
<th>Analog Ratiometric 10 % to 90 % (V+ = 5.0 V) (TSic x03)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-50 1)</td>
<td>0x000</td>
<td>0.000</td>
<td>10 % V+ (0.5 V)</td>
</tr>
<tr>
<td>-10</td>
<td>0x199</td>
<td>0.200</td>
<td>26 % V+ (1.3 V)</td>
</tr>
<tr>
<td>0</td>
<td>0x200</td>
<td>0.250</td>
<td>30 % V+ (1.5 V)</td>
</tr>
<tr>
<td>25</td>
<td>0x2FF</td>
<td>0.375</td>
<td>40 % V+ (2.0 V)</td>
</tr>
<tr>
<td>60</td>
<td>0x465</td>
<td>0.550</td>
<td>54 % V+ (2.7 V)</td>
</tr>
<tr>
<td>125</td>
<td>0x6FE</td>
<td>0.875</td>
<td>80 % V+ (4.0 V)</td>
</tr>
<tr>
<td>150 2)</td>
<td>0x7FF</td>
<td>1.000</td>
<td>90 % V+ (4.5 V)</td>
</tr>
</tbody>
</table>

1) LT = -50  2) HT = 150 as standard value for the temperature calculation

### Formulas for the output signal [°C]:

Analog output (0 V to 1 V):

\[ T = \frac{\text{Sig} [V]}{V^+ [V]} \times (\text{HT} - \text{LT}) + \text{LT} [°C] \]

Ratiometric output (10 % to 90 %):

\[ T = \frac{0.8 \times \text{Digital signal}}{\text{V}^+ [V]} \times (\text{HT} - \text{LT}) + \text{LT} [°C] \]

Digital output - 11 bit:

\[ T = \frac{\text{Digital signal}}{2047} \times (\text{HT} - \text{LT}) + \text{LT} [°C] \]

Digital output - 14 bit (TSic 316):

\[ T = \frac{\text{Digital signal}}{16384} \times (\text{HT} - \text{LT}) + \text{LT} [°C] \]

LT: Lower temperature limit [= -50 °C]  V+: Supply voltage [V]  
HT: Higher temperature limit [= +150 °C]  Sig[V]: Analog/ratiometric output signal [V]
The TSic™ series of temperature sensor ICs are specifically designed as a low-power solution for temperature measurement in building automation, medical / pharma technologies, industrial and mobile applications. The TSic™ provides a simple temperature measurement and achieves outstanding accuracy combined with long term stability.

The TSic™ has a high precision bandgap reference with a PTAT (proportional-to-absolute-temperature) output, a low-power and high-precision ADC and an on-chip DSP core with an EEPROM for the precisely calibrated output signal. The TSic™ temperature sensor is fully calibrated, meaning no further calibration effort is required by the customer. With an accuracy of ±0.1 K in a range of 40 K (e.g. +5 °C to +45 °C), the sensor is more accurate than a class F0.1 (DINEN 60751) platinum sensor.

Extended long wires (> 10 m) will not influence the accuracy. The TSic™ is available with digital (ZacWire, TSic™ 506F), analog (0 V to 1 V, TSic™ 501F) or ratiometric (10 % to 90 % V, TSic™ 503F) output signal. The low power consumption of about 35 µA makes it suitable for many applications.

### Output examples

<table>
<thead>
<tr>
<th>Temp (°C)</th>
<th>Digital Values (TSic x06)</th>
<th>Analog 0 V to 1 V (TSic x01)</th>
<th>Analog Ratiometric 10 % to 90 % (V+ = 5.0 V) (TSic x03)</th>
</tr>
</thead>
<tbody>
<tr>
<td>&lt; -10 to -10°</td>
<td>0x000</td>
<td>0.000</td>
<td>10 % V+ (0.5 V)</td>
</tr>
<tr>
<td>0</td>
<td>0x124</td>
<td>0.143</td>
<td>21.4 % V+ (1.07 V)</td>
</tr>
<tr>
<td>25</td>
<td>0x3FF</td>
<td>0.500</td>
<td>50 % V+ (2.5 V)</td>
</tr>
<tr>
<td>+60° to +60</td>
<td>0x7FF</td>
<td>1.000</td>
<td>90 % V+ (4.5 V)</td>
</tr>
</tbody>
</table>

1) LT = -10
2) HT = 60 as standard value for the temperature calculation

Formulas for the output signal [°C]:

**Analog output (0 V to 1 V):**

\[
T = \frac{\text{Sig}[V]}{V^+ [V]} - 0.1 \times (\text{HT} - \text{LT}) + \text{LT} [°C]
\]

**Ratiometric output (10 % to 90 %):**

\[
T = \frac{\text{Sig}[V]}{V^+ [V]} \times 0.8 \times (\text{HT} - \text{LT}) + \text{LT} [°C]
\]

**Digital output - 11 bit:**

\[
T = \frac{\text{Digital signal}}{2047} \times (\text{HT} - \text{LT}) + \text{LT} [°C]
\]

**Digital output - 14 bit (TSic 516):**

\[
T = \frac{\text{Digital signal}}{16384} \times (\text{HT} - \text{LT}) + \text{LT} [°C]
\]

LT: Lower temperature limit [= -10 °C]

HT: Higher temperature limit [= +60 °C]

V+: Supply voltage [V]

Sig[V]: Analog/ratiometric output signal [V]
3. **TSic™-716**

The TSic™ series of temperature sensor ICs are specifically designed as a low-power solution for temperature measurement in building automation, medical/pharma technologies, industrial and mobile applications. The TSic™ provides a simple temperature measurement and achieves outstanding accuracy combined with long term stability. The TSic™ has a high precision bandgap reference with a PTAT (proportional-to-absolute-temperature) output, a low-power and high-precision ADC and an on-chip DSP core with an EEPROM for the precisely calibrated output signal.

The IST TSic™ sensor is fully tested and calibrated to ensure the guaranteed accuracy. The TSic™ provides a simple temperature measurement and achieves outstanding accuracy combined with long term stability.

### Output examples

<table>
<thead>
<tr>
<th>Temp (°C)</th>
<th>Digital</th>
</tr>
</thead>
<tbody>
<tr>
<td>+35</td>
<td>0x2925</td>
</tr>
<tr>
<td>+40</td>
<td>0x2DB7</td>
</tr>
<tr>
<td>+45</td>
<td>0x3249</td>
</tr>
</tbody>
</table>

Formulas for the output signal [°C]:

\[
T = \frac{\text{Digital signal}}{16384} \times (HT - LT) + LT \quad [°C]
\]

**LT**: Lower temperature limit [\(= -10 \, °C\)]
**HT**: Higher temperature limit [\(= +60 \, °C\)]
**V**: Supply voltage [V]

4. **TSic™ Accuracy Overview**

<table>
<thead>
<tr>
<th>Product</th>
<th>Resolution</th>
<th>Range 1</th>
<th>Accuracy 1</th>
<th>Range 2</th>
<th>Accuracy 2</th>
<th>Range 3</th>
<th>Accuracy 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSic 20x</td>
<td>0.1 °C</td>
<td>+10 °C to +90 °C</td>
<td>±0.5 °C</td>
<td>-20 °C to +110 °C</td>
<td>±1 °C</td>
<td>-50 °C to +150 °C</td>
<td>±2 °C</td>
</tr>
<tr>
<td>TSic 30x</td>
<td>0.1 °C</td>
<td>+10 °C to +90 °C</td>
<td>±0.3 °C</td>
<td>-20 °C to +110 °C</td>
<td>±0.6 °C</td>
<td>-50 °C to +150 °C</td>
<td>±1.2 °C</td>
</tr>
<tr>
<td>TSic 50x</td>
<td>0.034 °C</td>
<td>+5 °C to +45 °C</td>
<td>±0.1 °C</td>
<td>-5 °C to +5 °C</td>
<td>±0.2 °C</td>
<td>+45 °C to +55 °C</td>
<td>±0.2 °C</td>
</tr>
<tr>
<td>TSic 716</td>
<td>0.034 °C</td>
<td>+25 °C to +45 °C</td>
<td>±0.07 °C</td>
<td>-</td>
<td>-</td>
<td>-10 °C to +60 °C</td>
<td>±0.2 °C</td>
</tr>
</tbody>
</table>

1) Range 1 can be shifted to a customer specific temperature
5. **ZACwire™ Digital Output**

### 5.1 TSi™ ZACwire™ Communication Protocol

ZACwire™ is a single wire bi-directional communication protocol. The bit encoding is similar to Manchester in that clocking information is embedded into the signal (falling edges of the signal happen at regular periods). This allows the protocol to be largely insensitive to baud rate differences between the two ICs communicating. In end-user applications, the TSi™ will be transmitting temperature information, and another IC in the system (most likely a µController) will be reading the temperature data over the ZACwire™.

### 5.2 Temperature Transmission Packet from a TSi™

The TSi™ transmits 1-byte packets. These packets consist of a start bit, 8 data bits, and a parity bit. The nominal baud rate is 8 kHz (125 µsec bit window). The signal is normally high. When a transmission occurs, the start bit occurs first followed by the data bits (MSB first, LSB last). The packet ends with an even parity bit.

![Figure 1.1 – ZACwire™ Transmission Packet](image_url)

The TSi™ provides temperature data with 11-bit or 14-bit resolution, and obviously these 11 bits or 14-bit of information cannot be conveyed in a single packet. A complete temperature transmission from the TSi™ consists of two packets. The first packet contains the most significant 3 bits or 6-bits of temperature information, and the second packet contains the least significant 8 bits of temperature information. There is a single bit window of high signal (stop bit) between the end of the first transmission and the start of the second transmission.

![Figure 1.2 – Full ZACwire™ Temperature Transmission from TSi™](image_url)

### 5.3 Bit Encoding

The bit format is duty cycle encoded:

- Start bit => 50 % duty cycle used to set up strobe time
- Logic 1 => 75 % duty cycle
- Logic 0 => 25 % duty cycle
Perhaps the best way to show the bit encoding is with an oscilloscope trace of a ZACwire™ transmission. The following shows a single packet of 96 Hex being transmitted. Because 96 Hex is already even parity, the parity bit is zero.

![Figure 1.3 – ZACwire™ Transmission](image)

5.4 How to Read a Packet

When the falling edge of the start bit occurs, measure the time until the rising edge of the start bit. This time ($T_{strobe}$) is the strobe time. When the next falling edge occurs, wait for a time period equal to $T_{strobe}$ and then sample the ZACwire™ signal. The data present on the signal at this time is the bit being transmitted. Because every bit starts with a falling edge, the sampling window is reset with every bit transmission. This means errors will not accrue for bits downstream from the start bit, as it would with a protocol such as RS232. It is recommended, however, that the sampling rate of the ZACwire™ signal when acquiring the start bit be at least 16x the nominal baud rate. Because the nominal baud rate is 8 kHz, a 128 kHz sampling rate is recommended when acquiring $T_{strobe}$.

5.5 How to Read a Packet using a µController

It is best to connect the ZACwire™ signal to a pin of the µController that is capable of causing an interrupt on a falling edge. When the falling edge of the start bit occurs, it causes the µController to branch to its ISR. The ISR enters a counting loop incrementing a memory location ($T_{strobe}$) until it sees a rise on the ZACwire™ signal. When $T_{strobe}$ has been acquired, the ISR can simply wait for the next 9 falling edges (8-data, 1-parity). After each falling edge, it waits for $T_{strobe}$ to expire and then sample the next bit.

The ZACwire™ line is driven by a strong CMOS push/pull driver. The parity bit is intended for use when the ZACwire™ is driving long (> 2 m) interconnects to the µController in a noisy environment. For systems in which the “noise environment is more friendly”, the user can choose to have the µController ignore the parity bit. In the appendix of this document is sample code for reading a TSic™ ZACwire™ transmission using a PIC16F627 µController.

5.6 How Often Does the TSic™ Transmit?

If the TSic™ is being read via an ISR, how often is it interrupting the µController with data? The update rate of the TSic™ can be programmed to one of 4 different settings: 250 Hz, 10 Hz, 1 Hz, and 0.1 Hz. This is done during calibration of the sensor on IST AG side. The standard update rate is 10 Hz (TSic 206, TSic 306, TSic 506) or 1 Hz (TSic 716). For other update rates please contact IST. Servicing a temperature-read ISR requires about 2.7 ms. If the update rate of the TSic™ is programmed to 250 Hz, then the µController spends about 66 % of its time reading the temperature transmissions. If, however, the update rate is programmed to something more reasonable like 1 Hz, then the µController spends about 0.27 % of its time reading the temperature transmissions.
5.7 Solutions if Real Time System Cannot Tolerate the TSic™ Interrupting the µController

Some real time systems cannot tolerate the TSic™ interrupting the µController. The µController must initiate the temperature read. This can be accomplished by using another pin of the µController to supply $V_{DD}$ to the TSic™. The TSic™ will transmit its first temperature reading approximately 65-85 ms ($T_R$) after power up. When the µController wants to read the temperature, it first powers the TSic™ using one of its port pins. It will receive a temperature transmission approximately 65 ms to 85 ms later. If during that 85 ms, a higher priority interrupt occurs, the µController can simply power down the TSic™ to ensure it will not cause an interrupt or be in the middle of a transmission when the high priority ISR finishes. This method of powering the TSic™ has the additional benefit of acting like a power down mode and reducing the quiescent current from a nominal 45 µA to zero. The TSic™ is a mixed signal IC and provides best performance with a clean $V_{DD}$ supply. Powering through a µController pin does subject it to the digital noise present on the µController's power supply. Therefore it is best to use a simple RC filter when powering the TSic™ with a µController port pin. See the diagram below.

1) This value is depending on the temperature. In lower temperatures this value can be lower too.

5.8 Appendix A: An Example of PIC1 Assembly Code for Reading the ZACwire™

In the following code example, it is assumed that the ZACwire™ pin is connected to the interrupt pin (PORTB, 0) of the PIC and that the interrupt is configured for falling edge interruption. This code should work for a PIC running between 2 MHz to 12 MHz.

```
TEMP_HIGH EQU 0X24 ;; MEMORY LOCATION RESERVED FOR TEMP HIGH BYTE
TEMP_LOW EQU 0X25 ;; MEMORY LOCATION RESERVED FOR TEMP LOW BYTE
LAST_LOC EQU 0X26 ;; THIS BYTE MUST BE CONSECUTIVE FROM TEMP_HIGH
TSTROBE EQU 0X26 ;; LOCATION TO STORE START BIT STROBE TIME
ORG  0X004  ;; ISR LOCATION

;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
CODE TO SAVE ANY NEEDED STATE AND TO DETERMINE THE SOURCE OF THE ISR GOES HERE. ONCE YOU HAVE DETERMINED THE SOURCE IF THE INTERRUPT WAS A ZAC WIRE TRANSMISSION THEN YOU BRANCH TO ZAC_TX

;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
ZAC_TX:                MOVLW TEMP_HIGH          ;; MOVE ADDRESS OF TEMP_HIGH (0X24) TO W REG
                    MOVWF FSR                      ;; FSR = INDIRECT POINTER, NOW PointING TO TEMP_HIGH
GET_TLOW:               MOVLW 0X02             ;; START TSTROBE COUNTER AT 02 TO ACCOUNT FOR
                    MOVWF TSTROBE                 ;; OVERHEAD IN GETTING TO THIS POINT OF ISR
                    CLRF INDF                    ;; CLEAR THE MEMORY LOCATION POINTED TO BY FS
```

---

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STRB:  
INCF  TSTROBE,1  ;; INCREMENT TSTROBE
BTFSC  STATUS,Z  ;; IF TSTROBE OVERFLOWED TO ZERO THEN
GOTO  RTI  ;; SOMETHING WRONG AND RETURN FROM INTERRUPT
BTFSS  PORTB,0  ;; LOOK FOR RISE ON ZAC WIRE
GOTO  STRB  ;; IF RISE HAS NOT YET HAPPENED INCREMENT TSTROBE

BIT_LOOP:  
CLRF  BIT_CNT  ;; MEMORY LOCATION USED AS BIT COUNTER
CLRF  STRB_CNT  ;; MEMORY LOCATION USED AS STROBE COUNTER
CLRF  TIME_OUT  ;; MEMORY LOCATION USED FOR EDGE TIME OUT

WAIT_FALL:  
BTFSS  PORTB,0  ;; WAIT FOR FALL OF ZAC WIRE
GOTO  PAUSE_STRB  ;; NEXT FALLING EDGE OCCURRED
INCFSZ  TIME_OUT,1  ;; CHECK IF EDGE TIME OUT COUNTER OVERFLOWED
GOTO  WAIT_FALL  ;; EDGE TIME OUT OCCURRED

PAUSE_STRB:  
INCF  STRB_CNT,1  ;; INCREMENT THE STROBE COUNTER
MOVF  TSTROBE,0  ;; MOVE TSTROBE TO W REG
SUBWF  STRB_CNT,0  ;; COMPARE STRB_CNT TO TSTROBE
BTFSS  STATUS,Z  ;; IF EQUAL THEN IT IS TIME TO STROBE
GOTO  PAUSE_STRB  ;; ZAC WIRE FOR DATA, OTHERWISE KEEP COUNTING
;; LENGTH OF THIS LOOP IS 6-STATES. THIS HAS TO
;; MATCH THE LENGTH OF THE LOOP THAT ACQUIRED TSTROBE
BCF  STATUS,C  ;; CLEAR THE CARRY
BTFSC  PORTB,0  ;; SAMPLE THE ZAC WIRE INPUT
BSF  STATUS,C  ;; IF ZAC WIRE WAS HIGH THEN SET THE CARRY
RLF  INDF,1  ;; ROTATE CARRY=ZAC WIRE INTO LSB OF REGISTER
;; THAT FSR CURRENTLY POINTS TO
CLRF  TIME_OUT  ;; CLEAR THE EDGE TIMEOUT COUN

WAIT_RISE:  
BTFSC  PORTB,0  ;; IF RISE HAS OCCURRED THEN WE ARE DONE
GOTO  NEXT_BIT  ;; EDGE TIME OUT OCCURRED.
INCFSZ  TIME_OUT,1  ;; INCREMENT EDGE TIME OUT COUNTER
GOTO  WAIT_RISE  ;; EDGE TIME OUT OCCURRED.

NEXT_BIT:  
INCF  BIT_CNT,1  ;; INCREMENT BIT COUNTER
MOVLW  0x08  ;; THERE ARE 8-BITS OF DATA
SUBWF  BIT_CNT,0  ;; TEST IF BIT COUNTER AT LIMIT
BTFSS  STATUS,Z  ;; IF NOT ZERO THEN GET NEXT BIT
GOTO  BIT_LOOP  ;; EDGE TIME OUT OCCURRED.

WAIT_PF:  
BTFSS  PORTB,0  ;; WAIT FOR FALL OF PARITY
GOTO  P_RISE  ;; EDGE TIME OUT OCCURRED
INCFSZ  TIME_OUT,1  ;; INCREMENT TIME_OUT COUNTER
GOTO  WAIT_PF  ;; EDGE TIME OUT OCCURRED

P_RISE:  
CLRF  TIME_OUT  ;; CLEAR THE EDGE TIME OUT COUNTER
GOTO  WAIT_PR  ;; WAIT FOR RISE OF PARITY

WAIT_PR:  
BTFSC  PORTB,0  ;; INCREMENT EDGE TIME OUT COUNTER
GOTO  NEXT_BYTE  ;; EDGE TIME OUT OCCURRED
INCFSZ  TIME_OUT,1  ;; INCREMENT EDGE TIME OUT COUNTER
GOTO  WAIT_PR  ;; EDGE TIME OUT OCCURRED
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NEXT_BYTE:
INCF FSR,1 ;; INCREMENT THE INDF POINTER
MOVLW LAST_LOC
SUBWF FSR,0 ;; COMPARE FSR TO LAST_LOC
BTFSS STATUS,Z ;; IF EQUAL THEN DONE
GOTO WAIT_TLOW

;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
; ; IF HERE YOU ARE DONE READING THE ZAC WIRE AND HAVE THE DATA ;;
; ; IN TEMP_HIGH & TEMP_LOW ;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;

WAIT_TLOW: CLRF TIME_OUT

WAIT_TLF:
BTFSS PORTB,0 ; WAIT FOR FALL OF PORTB,0 INDICATING
GOTO GET_TLOW ; START OF TEMP LOW BYTE
INCFSZ TIME_OUT
GOTO WAIT_TLF
GOTO RTI ; EDGE TIMEOUT OCCURRED

RTI:
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
; ; RESTORE ANY STATE SAVED OFF AT BEGINNING OF ISR ;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
BCF INTCON,INTF ;; CLEAR INTERRUPT FLAG
BSF INTCON,INTE ;; ENSURE INTERRUPT RE-ENABLED
RETFIE ;; RETURN FROM INTERRUPT

;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
6. Die and Package Specifications

6.1 SOP-8

The following dimensional drawings are for the TSic™ Series SOP-8 (SOIC Narrow, 0.150) package. See Table 1.1 and Table 1.2 on the next page for the dimensions labeled in these diagrams. Unless specified otherwise, dimensions are in inches.

Notes:
1. Maximum thickness allowed is 0.015
2. Dimensioning and tolerances:

<table>
<thead>
<tr>
<th>Decimal</th>
<th>Angular</th>
<th>3rd Angle Projection</th>
</tr>
</thead>
<tbody>
<tr>
<td>.xx ±0.01”</td>
<td>±1 °C</td>
<td></td>
</tr>
<tr>
<td>.xxx ±0.002”</td>
<td></td>
<td></td>
</tr>
<tr>
<td>.xxxx ±0.0010”</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

3. “T” is a reference datum
4. “D” & “E” are reference datums and do not include mold flash or protrusions but do include mold mismatch and are measured at the mold parting line. Mold flash and protrusions do not exceed 0.006 inches at the end and 0.01 “ at the window
5. “L” is the length of the terminal for soldering to a substrate
6. “N” is the number of terminal positions
7. Terminal positions are shown for reference only
8. Formed leads are planar with respect to one another within 0.03 “ at the seating plane
9. The appearance of the pin 1 marker is optionally either the round type or the rectangular type
10. Country of origin location on package bottom is optional and depends on assembly location
11. Controlling dimension: Inches
12. This part is compliant with JEDEC Standard MS-012, Variation AA, AB & AC

6.1.1 SOP-8 Pin Assignment

<table>
<thead>
<tr>
<th>Pin</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>V+</td>
<td>Supply voltage (3 V to 5.5 V)</td>
</tr>
<tr>
<td>2</td>
<td>Signal</td>
<td>Temperature output signal</td>
</tr>
<tr>
<td>3</td>
<td>Gnd</td>
<td>Ground</td>
</tr>
<tr>
<td>4</td>
<td>TP/NC</td>
<td>Test pin / NC Do not connect</td>
</tr>
</tbody>
</table>
### 6.1.2 Inches

<table>
<thead>
<tr>
<th>Dimension</th>
<th>Note</th>
<th>Variations</th>
<th>Note</th>
<th>Variations</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>MIN</td>
<td>0.061</td>
<td>NOM</td>
<td>0.064</td>
</tr>
<tr>
<td>A1</td>
<td>MIN</td>
<td>0.004</td>
<td>NOM</td>
<td>0.006</td>
</tr>
<tr>
<td>A2</td>
<td>MIN</td>
<td>0.055</td>
<td>NOM</td>
<td>0.058</td>
</tr>
<tr>
<td>B</td>
<td>MIN</td>
<td>0.0138</td>
<td>NOM</td>
<td>0.016</td>
</tr>
<tr>
<td>C</td>
<td>MIN</td>
<td>0.0075</td>
<td>NOM</td>
<td>0.008</td>
</tr>
<tr>
<td>D</td>
<td>MIN</td>
<td>See variations</td>
<td>NOM</td>
<td>3</td>
</tr>
<tr>
<td>E</td>
<td>MIN</td>
<td>0.15</td>
<td>NOM</td>
<td>0.155</td>
</tr>
<tr>
<td>e</td>
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<td>MIN</td>
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<td>NOM</td>
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### 6.1.3 Millimeters

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<th>Variations</th>
<th>Note</th>
<th>Variations</th>
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6.2 TO92

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6.2.1 TO92 Pin Assignment

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<th>Name</th>
<th>Description</th>
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</thead>
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<td>3</td>
<td>V+ (VDD)</td>
<td>Supply Voltage (3 V to 5.5 V)</td>
</tr>
<tr>
<td>2</td>
<td>Signal</td>
<td>Temperature Output Signal</td>
</tr>
<tr>
<td>1</td>
<td>Gnd (VSS)</td>
<td>Ground</td>
</tr>
</tbody>
</table>

6.3 Bare Die

Pad positions:

- 0.2158 mm
- 0.2662 mm
- 0.5249 mm
- 0.6515 mm
- 0.997 mm

1.372 mm (pad positions)
1.61 mm
6.3.1 Bare Die Pin Assignment

<table>
<thead>
<tr>
<th>Pin</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>V+ (V_{DD})</td>
<td>Supply Voltage (3 V to 5.5 V)</td>
</tr>
<tr>
<td>2</td>
<td>Signal</td>
<td>Temperature Output Signal</td>
</tr>
<tr>
<td>1</td>
<td>Gnd (V_{SS})</td>
<td>Ground</td>
</tr>
</tbody>
</table>

Die Thickness: 390 µm
Pad size: 68 µm x 68 µm

The analog and digital power and ground of the chip are wired to same substrate or Flex-Pad: V_{DDA} and V_{DD} are wired to V_{DD}, and V_{SSA} and V_{SS} are wired to Ground. The Signal pin needs only one wire.

13. TSic™ Block Diagram

[Block diagram image]

The analog and digital power and ground of the chip are wired to same substrate or Flex-Pad: V_{DDA} and V_{DD} are wired to V_{DD}, and V_{SSA} and V_{SS} are wired to Ground. The Signal pin needs only one wire.